

U.S. Serial No. 10/765,027

Response to the Office action of September 19, 2005

This listing of claims will replace all prior versions, and listings, of claims in the application;

The Status of the Claims

1. (Previously Presented) A method for manufacturing a MOSFET device, the method comprising:
- (a) selectively forming a shallow trench isolation in a substrate;
 - (b) forming a first oxide layer on a surface of an active region of the substrate and implanting ions therein for forming a low doped drain in the active region prior to the formation of a gate;
 - (c) forming a first nitride layer;
 - (d) removing a part of the first nitride layer and the oxide layer where the gate will be located and etching the substrate corresponding to the part by a predetermined depth;
 - (e) forming a second oxide layer over an exposed portion of the substrate;
 - (f) implanting ions into the substrate;
 - (g) removing the second oxide layer;
 - (h) depositing a gate insulating layer and a polysilicon layer;
 - (i) polishing until the first nitride layer is exposed;
 - (j) removing the first nitride layer, depositing an oxide layer conformally and depositing a second nitride layer;
 - (k) etching the second nitride layer to form a gate sidewall of nitride;
 - (l) implanting ions into the substrate to form a source and drain at both sides of the gate; and
 - (m) removing an exposed oxide layer.

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2. (Original) A method as defined by claim 1, wherein the substrate comprises a silicon substrate.

3. (Original) A method as defined by claim 1, wherein the shallow trench isolation comprises an oxide layer.

4. (Original) A method as defined by claim 1, wherein the predetermined depth is in range of about 200 to about 1000 angstroms.

5. (Original) A method as defined by claim 1, wherein the exposed substrate is oxidized at about 600 to about 800 °C to form the second oxide layer having a thickness of about 100 angstroms in (e).

6. (Original) A method as defined by claim 1, wherein a chemical mechanical polishing is performed in (i).

7. (Previously Presented) A method as defined by claim 1, wherein the second nitride layer is removed by an etch back processing in (k).